Abstract

A processor includes controller circuitry configurable to determine for a given packet or other protocol data unit (PDU) received by the processor whether the given PDU is a single-cell PDU. If the given PDU is a single-cell PDU, information characterizing the given PDU is stored in first memory circuitry internal to the processor, without utilizing a linked list data structure. If the given PDU is not a single-cell PDU, information characterizing the PDU is stored in second memory circuitry external to the processor, utilizing a linked list data structure. The processor may be configured as a network processor integrated circuit to provide an interface between a network and a switch fabric in a router or switch.